ABSTRACT

Embodiments include a semiconductor device including a non-volatile memory transistor with a split-gate structure that is operable at a lower voltage. The semiconductor device includes a P-type silicon substrate 10 that includes a memory region 4000, an N-type first well 11 located in the memory region 4000, and a P-type second well located in the first well 11. The semiconductor device includes a non-volatile memory transistor with a split-gate structure. A source 16 and a drain 14 of the non-volatile memory transistor are located in the second well 12. The silicon substrate 10 and the second well 12 are isolated from each other by the first well 11. Therefore, the potential of the second well 12 can be set independently of the potential of the silicon substrate 11.